

Application No. 10/757,750
Amendment dated March 13, 2006
After Final Office Action of January 23, 2006

2

Docket No.: 08211/0200349-US0 (P05782)

AMENDMENTS TO THE CLAIMS

Claims 1-25 (Canceled)

26. (Currently amended) A circuit for analog-to-digital conversion, comprising:
a fine channel circuit that includes folding stages;
a coarse channel circuit; and
a coarse channel calibration circuit that is coupled to the coarse channel circuit,
wherein the coarse channel calibration circuit includes:
a counter circuit that is coupled to the coarse channel circuit; and
a parameter adjustment circuit that is coupled to the counter circuit and the coarse
channel circuit, wherein
the coarse channel circuit is configured to provide a feedback signal,
the counter circuit is configured to:
receive the feedback signal, and
provide a count signal in response to the feedback signal, and wherein
the parameter adjustment circuit is configured to:
receive the count signal, and
adjust a parameter of the coarse channel circuit in response to the count signal, and
wherein the counter circuit is configured to, if latched:
increment a count value that is associated with the count signal if the comparator
output corresponds to a first logic level, and
decrement the count value if the comparator output corresponds to a second logic
level.
27. (Previously Presented) The circuit of Claim 26, further comprising:
a control circuit that is configured to provide a select signal; and
a voltage reference circuit that is configured to provide a voltage reference signal that
corresponds to the select signal, wherein
the coarse channel circuit is configured to receive the voltage reference signal.

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Application No. 10/757,750
Amendment dated March 13, 2006
After Final Office Action of January 23, 2006

3

Docket No.: 08211/0200349-US0 (P05782)

28. (Currently amended) The circuit of Claim 26,
wherein the coarse channel circuit is configured to provide an output signal in response to a voltage reference signal, and
~~wherein the coarse channel calibration circuit is configured to:~~
~~receive a feedback signal from the coarse channel circuit, and~~
~~provide an adjustment signal to the coarse channel circuit in response to the feedback signal.~~
29. (Previously Presented) The circuit of Claim 26,
wherein the coarse channel circuit comprises an amplifier array and a comparator array, and
wherein at least one of the amplifier array or the comparator array is configured to receive an adjustment signal.
30. (Previously Presented) The circuit of Claim 28,
wherein the output signal includes the feedback signal.
31. (Canceled)
32. (Currently amended) The circuit of Claim 26[[31]],
wherein the parameter adjustment circuit includes a digital-to-analog converter circuit, and
wherein the digital-to-analog converter circuit is configured to provide a converted signal to the coarse channel circuit.
33. (Canceled)

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Application No. 10/757,750
Amendment dated March 13, 2006
After Final Office Action of January 23, 2006

4

Docket No.: 08211/0200349-US0 (P05782)

34. (Currently amended) The circuit of Claim 26[[33]],
wherein the parameter comprises one of a single-ended current or differential current.

35. (Canceled)

36. (Currently amended) The circuit of Claim 33,A circuit for analog-to-digital conversion,

comprising:

a fine channel circuit that includes folding stages;

a coarse channel circuit; and

a coarse channel calibration circuit that is coupled to the coarse channel circuit,

wherein the coarse channel calibration circuit includes:

a counter circuit that is coupled to the coarse channel circuit; and

a parameter adjustment circuit that is coupled to the counter circuit and the coarse
channel circuit, wherein

the coarse channel circuit is configured to provide a feedback signal,

the counter circuit is configured to:

receive the feedback signal, and

provide a count signal in response to the feedback signal, and wherein

the parameter adjustment circuit is configured to:

receive the count signal, and

adjust a parameter of the coarse channel circuit in response to the count signal, and

wherein the parameter adjustment circuit includes:

a first digital-to-analog converter circuit that is configured to convert the count signal
into a first analog signal; and

a second digital-to-analog converter circuit that is configured to convert an inverted
count signal into a second analog signal.

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Application No. 10/757,750
Amendment dated March 13, 2006
After Final Office Action of January 23, 2006

5

Docket No.: 08211/0200349-US0 (P05782)

37. (Previously Presented) The circuit of Claim 36, wherein
the coarse channel circuit includes an amplifier that is configured to provide a differential
output current,

the amplifier includes:

a first load that is configured to receive a first half of the differential output current
and the first analog signal; and

a second load that is configured to receive a second half of the differential output
current and the second analog signal,

the first current digital-to-analog converter circuit is configured to provide the first analog
signal to the first load, and wherein

the second current digital-to-analog converter circuit is configured to provide the second
analog signal to the second load.

38. (Previously Presented) The circuit of Claim 37, wherein
the first current digital-to-analog converter circuit includes:

a first current digital-to-analog converter; and

a first transistor that is coupled between the first current digital-to-analog converter
and the first load,

the second current digital-to-analog converter circuit includes:

a second current digital-to-analog converter; and

a second transistor that is coupled between the first current digital-to-analog
converter and the first load, and wherein

the first and second transistors are each configured to operate as cascode transistors.

39. (Currently amended) A circuit for analog-to-digital conversion, comprising:
a fine channel circuit that includes folding stages;
a coarse channel circuit;
a coarse channel calibration circuit that is coupled to the coarse channel circuit; and ~~The~~
~~circuit of Claim 26, further comprising:~~

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Application No. 10/757,750
Amendment dated March 13, 2006
After Final Office Action of January 23, 2006

6

Docket No.: 08211/0200349-US0 (P05782)

a control circuit that is configured to:

provide a select signal; and

provide a timing signal at a pre-determined amount of time after providing the select signal,

wherein the coarse channel circuit is configured to provide an output signal, and

wherein the coarse channel calibration circuit is configured to latch the output signal in response to the timing signal.

40. (Currently amended) A circuit for calibration in a folding analog-to-digital conversion architecture, the circuit comprising:

a coarse channel calibration circuit that is configured to:

receive an output signal from a coarse channel circuit of a folding analog-to-digital converter circuit; and

adjust a parameter of the coarse channel circuit in response to the output signal; and

a control circuit that is arranged to:

provide a select signal for selecting a voltage reference; and

assert a timing signal for latching the coarse channel calibration circuit at a pre-determined amount of time after a change of the select signal.

41. (Canceled)

42. (Previously Presented) The circuit of Claim 40,

wherein the coarse channel calibration circuit includes:

a counter circuit that is configured to provide a count signal in response to the timing signal and the output signal; and

a parameter adjustment circuit that is configured to adjust the parameter in response to the count signal.

Claims 43-45 (Canceled)

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Application No. 10/757,750
Amendment dated March 13, 2006
After Final Office Action of January 23, 2006

7

Docket No.: 08211/0200349-US0 (P05782)

46. (Previously Presented) The circuit of Claim 26, wherein
the fine channel circuit is arranged to perform a fine analog-to-digital conversion of an input
signal; and
wherein the coarse channel circuit is arranged to perform a coarse analog-to-digital
conversion of the input signal in parallel with fine analog-to-digital conversion.
47. (Previously Presented) The circuit of Claim 26, wherein
the coarse channel circuit is arranged to perform a coarse analog-to-digital conversion; and
wherein the coarse channel calibration circuit is arranged to calibrate the coarse analog-to-
digital conversion.
48. (Previously Presented) The circuit of Claim 26,
wherein the coarse channel circuit includes an amplifier array.
49. (Currently amended) The circuit of Claim 29,
wherein the coarse channel calibration circuit is configured to:
~~receive a feedback signal from the coarse channel circuit, and~~
provide the adjustment signal to the coarse channel circuit in response to the
feedback signal.
50. (Canceled)
51. (Canceled)
52. (Currently amended) The circuit of ~~Claim 51, further comprising~~ A circuit for analog-to-
digital conversion, comprising:
a folding analog-to-digital converter, including:
a fine channel circuit that is coupled to an input node;

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Application No. 10/757,750
Amendment dated March 13, 2006
After Final Office Action of January 23, 2006

8

Docket No.: 08211/0200349-US0 (P05782)

a coarse channel circuit that is coupled to the input node;
a coarse channel calibration circuit that is coupled to the coarse channel circuit; and
an encoder circuit, wherein

the fine channel circuit is operable to provide a fine analog-to-digital conversion output signal by performing a fine analog-to-digital conversion on an input signal that is received at the input node;

the coarse channel circuit is operable to provide a coarse analog-to-digital conversion output signal by performing a coarse analog-to-digital conversion on the input signal;

the encoder circuit is operable to provide a digital output signal based on the coarse analog-to-digital conversion output signal and the fine analog-to-digital conversion output signal;

the coarse channel calibration circuit is operable to receive the coarse analog-to-digital output signal, and to provide an adjustment signal based on the coarse analog-to-digital output signal; and

wherein the coarse channel circuit includes:

a comparator array including a plurality of comparators, wherein

the comparator array is operable to receive the input signal and a plurality of coarse reference voltages, and to provide a plurality of comparator output signals;

the coarse analog-to-digital conversion output signal is the plurality of comparator output signals; and

wherein each of the plurality of comparators in the comparator array is arranged to: compare the input signal with a corresponding one of the plurality of coarse references voltages, and to provide a corresponding one of the plurality of comparator output signals based on the comparison.

53. (Currently amended) The circuit of Claim 51, further comprising A circuit for analog-to-digital conversion, comprising:

a folding analog-to-digital converter, including:

a fine channel circuit that is coupled to an input node;

a coarse channel circuit that is coupled to the input node;

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Application No. 10/757,750
Amendment dated March 13, 2006
After Final Office Action of January 23, 2006

9

Docket No.: 08211/0200349-US0 (P05782)

a coarse channel calibration circuit that is coupled to the coarse channel circuit; and
an encoder circuit, wherein

the fine channel circuit is operable to provide a fine analog-to-digital conversion output signal by performing a fine analog-to-digital conversion on an input signal that is received at the input node;

the coarse channel circuit is operable to provide a coarse analog-to-digital conversion output signal by performing a coarse analog-to-digital conversion on the input signal;

the encoder circuit is operable to provide a digital output signal based on the coarse analog-to-digital conversion output signal and the fine analog-to-digital conversion output signal;

the coarse channel calibration circuit is operable to receive the coarse analog-to-digital output signal, and to provide an adjustment signal based on the coarse analog-to-digital output signal; and

wherein the coarse channel circuit includes:

at least one amplifier array, wherein the at least one amplifier array is operable to provide a plurality of amplifier output signals based, at least in part, on the input signal;

a comparator array including a plurality of comparators, wherein

the coarse analog-to-digital conversion output signal is the plurality of comparator output signals; and

wherein the comparator array is operable to receive the plurality of amplifier output signals, and to provide a plurality of comparator output signals, wherein each of the plurality of comparator output signals is based on a comparison of the input signal to a corresponding one of the plurality of coarse reference voltages, and wherein the at least one amplifier array provides gain prior to the comparison.

54. (Currently amended) The circuit of Claim 51, further comprising A circuit for analog-to-digital conversion, comprising:

a folding analog-to-digital converter, including:

a fine channel circuit that is coupled to an input node;

a coarse channel circuit that is coupled to the input node;

{S:\08211\0200349-US0\80054457.DOC [REDACTED]}

Application No. 10/757,750
Amendment dated March 13, 2006
After Final Office Action of January 23, 2006

10

Docket No.: 08211/0200349-US0 (P05782)

a coarse channel calibration circuit that is coupled to the coarse channel circuit; and
an encoder circuit, wherein

the fine channel circuit is operable to provide a fine analog-to-digital conversion output signal by performing a fine analog-to-digital conversion on an input signal that is received at the input node;

the coarse channel circuit is operable to provide a coarse analog-to-digital conversion output signal by performing a coarse analog-to-digital conversion on the input signal;

the encoder circuit is operable to provide a digital output signal based on the coarse analog-to-digital conversion output signal and the fine analog-to-digital conversion output signal;

the coarse channel calibration circuit is operable to receive the coarse analog-to-digital output signal, and to provide an adjustment signal based on the coarse analog-to-digital output signal;

the coarse channel circuit includes:

a comparator array including a plurality of comparators, wherein

the comparator array is operable to receive the input signal and a plurality of coarse reference voltages, and to provide a plurality of comparator output signals;

the coarse analog-to-digital conversion output signal is the plurality of comparator output signals; and

wherein each of the plurality of comparators in the comparator array is arranged to: compare the input signal with a corresponding one of the plurality of coarse references voltages, and to provide a corresponding one of the plurality of comparator output signals based on the comparison;

the comparator array is operable to receive the adjustment signal; and

wherein the comparator array is configured such that a parameter of the comparator array is adjusted based on the adjustment signal.

55. (Currently amended) The circuit of Claim 51, further comprisingA circuit for analog-to-digital conversion, comprising:

a folding analog-to-digital converter, including:

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Application No. 10/757,750
Amendment dated March 13, 2006
After Final Office Action of January 23, 2006

11

Docket No.: 08211/0200349-US0 (P05782)

a fine channel circuit that is coupled to an input node;
a coarse channel circuit that is coupled to the input node;
a coarse channel calibration circuit that is coupled to the coarse channel circuit; and
an encoder circuit, wherein

the fine channel circuit is operable to provide a fine analog-to-digital conversion output signal by performing a fine analog-to-digital conversion on an input signal that is received at the input node;

the coarse channel circuit is operable to provide a coarse analog-to-digital conversion output signal by performing a coarse analog-to-digital conversion on the input signal;

the encoder circuit is operable to provide a digital output signal based on the coarse analog-to-digital conversion output signal and the fine analog-to-digital conversion output signal;

the coarse channel calibration circuit is operable to receive the coarse analog-to-digital output signal, and to provide an adjustment signal based on the coarse analog-to-digital output signal;

the coarse channel circuit includes:

at least one amplifier array, wherein the at least one amplifier array is operable to provide a plurality of amplifier output signals based, at least in part, on the input signal;

a comparator array including a plurality of comparators, wherein

the coarse analog-to-digital conversion output signal is the plurality of comparator output signals;

the comparator array is operable to receive the plurality of amplifier output signals, and to provide a plurality of comparator output signals, wherein each of the plurality of comparator output signals is based on a comparison of the input signal to a corresponding one of the plurality of coarse reference voltages, and wherein the at least one amplifier array provides gain prior to the comparison;

the comparator array is operable to receive the adjustment signal; and

wherein the comparator array is configured such that a parameter of the comparator array is adjusted based on the adjustment signal.

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Application No. 10/757,750
Amendment dated March 13, 2006
After Final Office Action of January 23, 2006

12

Docket No.: 08211/0200349-US0 (P05782)

56. (Currently amended) The circuit of Claim 51, further comprising A circuit for analog-to-digital conversion, comprising:

a folding analog-to-digital converter, including:

a fine channel circuit that is coupled to an input node;

a coarse channel circuit that is coupled to the input node;

a coarse channel calibration circuit that is coupled to the coarse channel circuit; and

an encoder circuit, wherein

the fine channel circuit is operable to provide a fine analog-to-digital conversion output signal by performing a fine analog-to-digital conversion on an input signal that is received at the input node;

the coarse channel circuit is operable to provide a coarse analog-to-digital conversion output signal by performing a coarse analog-to-digital conversion on the input signal;

the encoder circuit is operable to provide a digital output signal based on the coarse analog-to-digital conversion output signal and the fine analog-to-digital conversion output signal;

the coarse channel calibration circuit is operable to receive the coarse analog-to-digital output signal, and to provide an adjustment signal based on the coarse analog-to-digital output signal;

the coarse channel circuit includes:

at least one amplifier array, wherein the at least one amplifier array is operable to provide a plurality of amplifier output signals based, at least in part, on the input signal;

a comparator array including a plurality of comparators, wherein

the coarse analog-to-digital conversion output signal is the plurality of comparator output signals;

the comparator array is operable to receive the plurality of amplifier output signals, and to provide a plurality of comparator output signals, wherein each of the plurality of comparator output signals is based on a comparison of the input signal to a corresponding one of the plurality of coarse reference voltages, and wherein the at least one amplifier array provides gain prior to the comparison; and

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Application No. 10/757,750
Amendment dated March 13, 2006
After Final Office Action of January 23, 2006

13

Docket No.: 08211/0200349-USO (P05782)

wherein at least one of the at least one amplifier array is operable to receive the adjustment signal such that a parameter of the at least one amplifier array in the at least one amplifier array is adjusted based on the adjustment signal.

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